CLAIMS:

1. A display device comprising:

- a cathode ray tube (T) having an electron gun (G) for generating at least one electron beam, and an outer conductive layer (AD);
- a video amplifier (VA) for modulating the at least one electron beam;
- video processing circuitry (VP) for providing a video signal (Vo) having a black level (BLR, BLG, BLB) to the video amplifier (VA) , the video processing circuitry (VP) comprising black level controlling circuitry (BL) for controlling the black level (BLR, BLG, BLB) of the video signal (Vo);
- a high-tension generator (H) having output terminals;
- and a sensing circuit (S) for sensing a black current level (IBR, IBG, IBB) of the at least one electron beam corresponding to the black level (BLR, BLG, BLB) of the video signal (Vo) and for feeding back information about the black current level (IBR, IBG, IBB) to the black level controlling circuitry (BL) for stabilizing the black current level (IBR, IBG, IBB),

the sensing circuit (S) being coupled to a node (X) to which the outer conductive layer (AD) and one of the output terminals of the high-tension generator (H) are coupled.

2. A display device as claimed in claim 1, wherein the sensing circuit (S) is coupled between the node (X) and a reference voltage source (V1).

3. A display device as claimed in claim 1, wherein the electron gun (G) is adapted for generating three electron beams; and the black level controlling circuitry (BL) is adapted for allowing the sensing circuit (S) to sequentially sense the black current levels (IBR, IBG, IBB) of each of the three beams.

4. A display device as claimed in claim 1, wherein the sensing circuit (S) comprises a current mirror circuit coupled between the node (X) and the reference voltage source (V1), an output of the current mirror circuit being coupled to the video processing circuitry (VP).

5. A display device as claimed in claim 4, wherein the current mirror circuit comprises:

- a first transistor (Q1) having a pair of first main terminals and a first control terminal, the first main terminals being coupled between the node (X) and the reference voltage source (V1) , the first control terminal being coupled to the node (X); and
- a second transistor (Q2) having a pair of second main terminals and a second control terminal, the second control terminal being coupled to the first control terminal, one of the second main terminals being coupled to the reference voltage source (V1) and the other of the second main terminals being coupled to the video processing circuitry (VP).